In the Claims:

1 . (Currently Amended) A method of manufacturing on a substrate a 2-transistor memory cell comprising a storage transistor having a memory gate stack and a selecting transistor, there being a tunnel dielectric layer between the substrate and the memory gate stack, the method comprising:

forming the memory gate stack by providing a first conductive layer and a second conductive layer and etching the second conductive layer thus forming a control gate and etching the first conductive layer thus forming a floating gate,

the method furthermore comprising,

before etching the first conductive layer, forming spacers against the control gate in the direction of a channel to be formed under the tunnel dielectric layer, the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers, and

thereafter using the spacers as a hard mask to etch the first conductive layer thus forming the floating gate.

2. (Cancelled).

3. (Currently Amended) A method according to ~~claim 2~~ claim 1, wherein the dielectric material having an oxygen diffusion through the material that is an order of magnitude smaller than oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or metal oxide.

4. (Previously presented) A method according to claim 1 , furthermore comprising,

before forming the memory gate stack, applying the tunnel dielectric layer on the substrate, and

after formation of the memory gate stack, removing the tunnel dielectric layer by a selective etching technique at least at a location where the selecting transistor is to be formed, the selective etching technique preferentially etching the tunnel dielectric layer compared to the substrate.

5. (Previously presented) A method according to claim 1, comprising,

after etching of the first conductive layer, providing a floating gate dielectric next to the formed floating gate and at the same time providing an access gate dielectric.

6. (Previously presented) A method according to claim 1, the memory gate stack comprising an interlayer dielectric layer between the first conductive layer and the second conductive layer, the method furthermore comprising

removing part of the interlayer dielectric layer after forming the control gate but before forming the spacers.

7. (Previously presented) A method according to claim 1 , the selecting transistor comprising an access gate, the method comprising

forming the access gate while the spacer at the access gate side is still present.

8. (Currently Amended) A 2-transistor memory cell comprising,

a storage transistor and

a selecting transistor, the storage transistor comprising a floating gate and a control gate, wherein the control gate is smaller than the floating gate, ~~and~~ spacers are present next to the control gate, and the spacers are made from a dielectric material having an oxygen diffusion through the dielectric material that is an order of magnitude smaller than oxygen diffusion through oxide spacers.

9. (Cancelled).

10. (Previously presented) A memory cell according to claim 8, the selecting transistor comprising an access gate, a spacer being present between the control gate and the access gate and a floating gate dielectric being present between the floating gate and the access gate, wherein the spacer is thicker than the floating gate dielectric

11. (Currently Amended) An electronic device comprising a 2-transistor memory cell including,

a storage transistor and

a selecting transistor, the storage transistor comprising a floating gate and a control gate, wherein the control gate is smaller than the floating gate, ~~and~~ spacers are present next to the control gate, and the spacers are made from a dielectric material having an oxygen diffusion through the dielectric material that, relative to oxide spacers, is an order of magnitude smaller than the oxygen diffusion through the oxide spacers.

12. (Cancelled).

13. (Currently Amended) The electronic device as recited in ~~claim 12~~ claim 11, wherein the selecting transistor includes,

an access gate,

a spacer being present between the control gate, and

the access gate and a floating gate dielectric being present between the floating gate and the access gate, wherein the spacer is thicker than the floating gate dielectric.